SILICON PHOTONICS packaging capability

company site Trutnov

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ARGOTECH

COMPLEX SOLUTION

PACKAGING DESIGN CAPABILITIES

- RF, thermal, optical, mechanical
- FEM and vector design tools

PROTOTYPING AND ASSEMBLY

- samples and prototypes assembly
- volume packaging
- die attach and wire bonding
- hybrid integration and optical coupling
- hermetic sealing

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PACKAGING APPROACHES

WAFER SCALE

- micro-assembly directly on the wafer level carriers or on PICs aggregated in the wafer

DISCRETE LEVEL

- integration on the PCB, TO-CAN, butterfly modules etc.

MICRO ASSEMBLY

DIE ATTACH

- both face up and face down (flip chip)
- accuracy up to +/-1um
- fixation adhesive, soldering, thermocompression

WIRE BONDING

- supporting all the WB techniques available of the shelve
- ball, wedge, BSOB, ribbon

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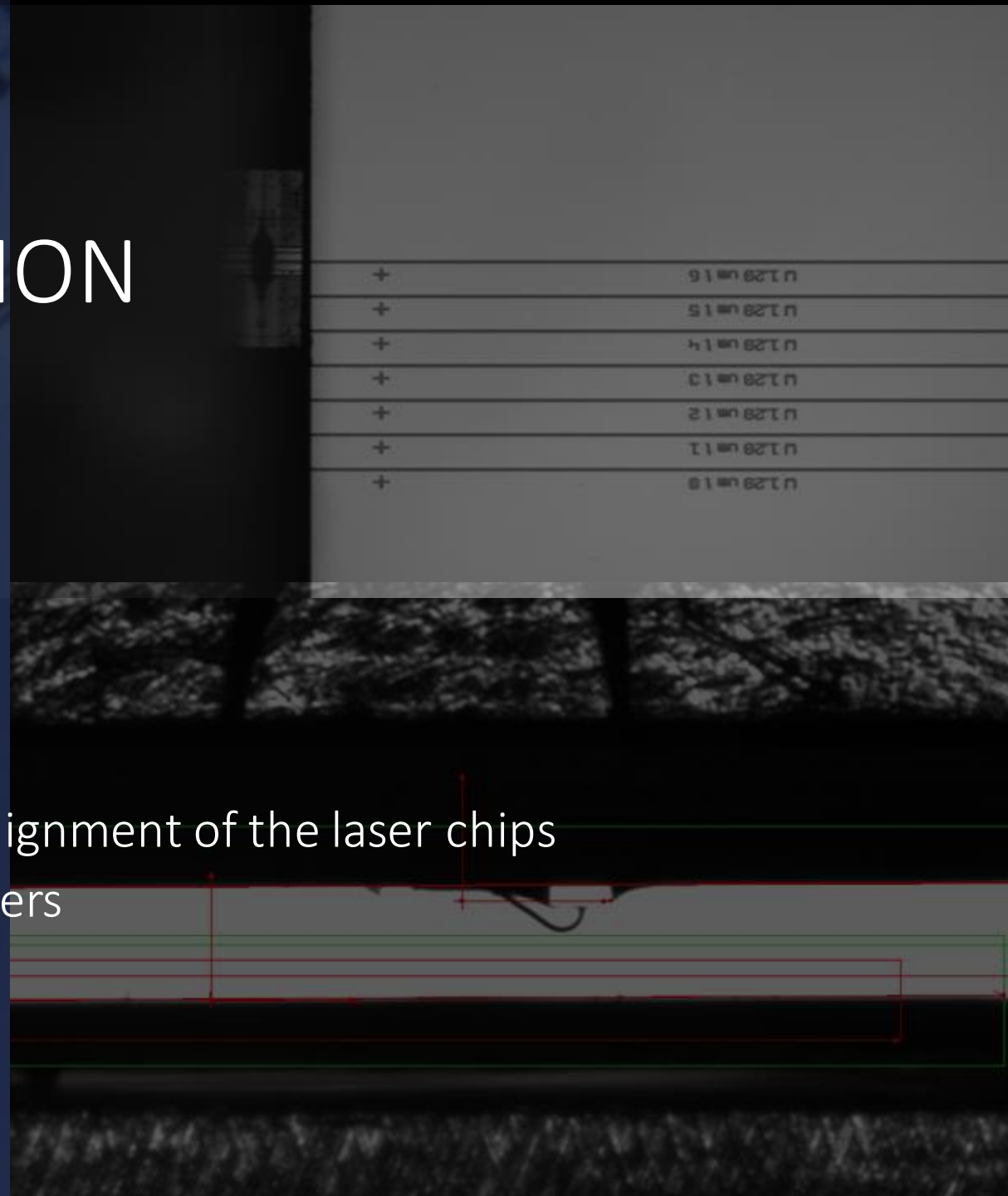
HYBRID INTEGRATION

CMOS CHIPS

- drivers, amplifiers, DACs etc.
- face down approach

III-V chips

- high accuracy flip chip or active alignment of the laser chips
- both VCSEL and edge emitting lasers



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OPTICAL COUPLING

FREE SPACE OPTICS COUPLING

- using lens elements in the optical path
- helps to deal with different MFD of chips and fiber in the application
- single mode and multi mode fibers
- wide spectrum experience from visible lasers (blue lasers into 2,5um fiber core), via near infrared (sensing and telecom spectrum) to mid infrared (QCL + PIC integration)

Active alignment technologies with 4 degree of freedom (DOF) with laser welding and adhesive based fixation

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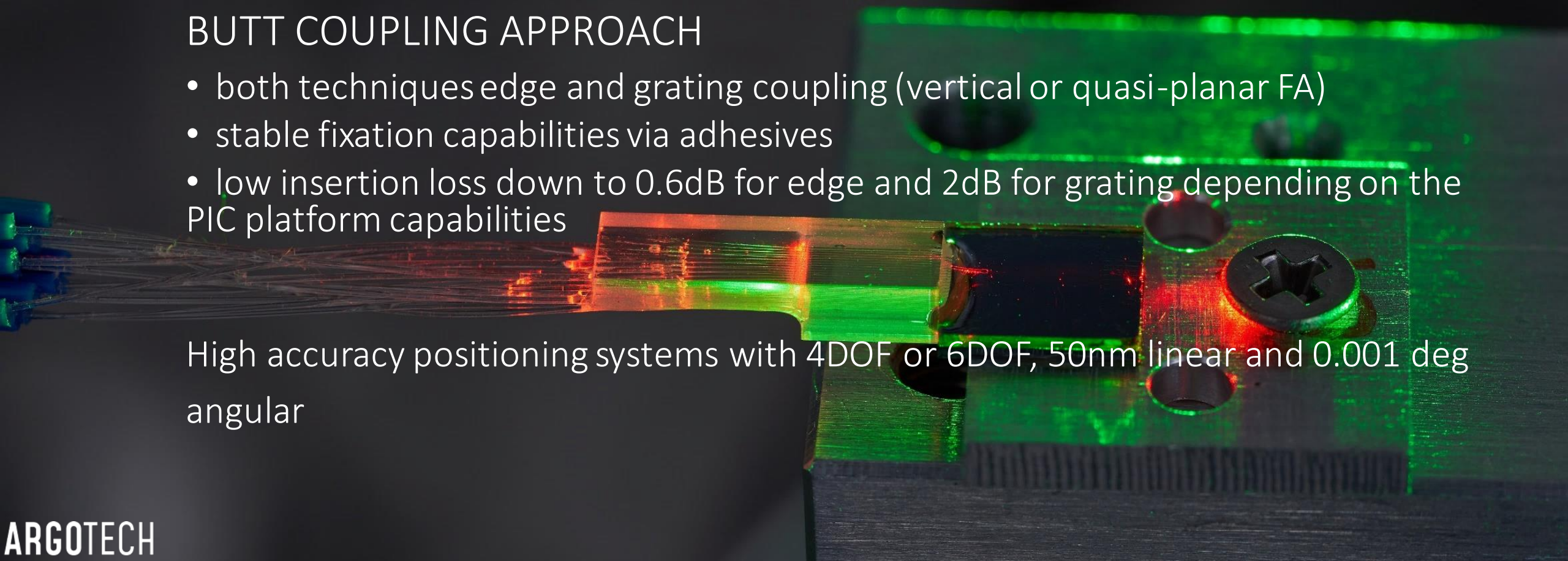
OPTICAL COUPLING

BUTT COUPLING APPROACH

- both techniques edge and grating coupling (vertical or quasi-planar FA)
- stable fixation capabilities via adhesives
- low insertion loss down to 0.6dB for edge and 2dB for grating depending on the PIC platform capabilities

High accuracy positioning systems with 4DOF or 6DOF, 50nm linear and 0.001 deg angular



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Qualification and tests

AGEING TEST

- lasers, LEDs, APDs
- effective platform based on the wafer scale carriers with high number of the chips under test (several thousands up to tens of thousands)

STANDARDS

- telcordia, JEDEC, MIL
- development cycle EVS-DVS-PVS


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